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Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	08/801,628
		Filing Date	08 March 2001
		First Named Inventor	Keeth et al.
		Group Art Unit	2818
		Examiner Name	Not yet assigned
		Attorney Docket Number	DB000575-010
Sheet	2	of	3

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
AKT		SUGIBAYASHI ET AL., "A 30-ns 256-Mb DRAM with a Multidivided Array Structure", IEEE Journal of Solid-State Circuits, Vol. 28 (No. 11), (November 1993)	
		TAGUCHI ET AL., "A 40-ns 64-Mb DRAM with 84-b Parallel Data Bus Architecture", IEEE Journal of Solid-State Circuits, Vol. 26 (No. 11), (November 1991)	
		KITSUKAWA ET AL., "256-Mb DRAM Circuit Technologies for File Applications", IEEE Journal of Solid-State Circuits, Vol. 28 (No. 11), (November 1993)	
		JEDEC SOLID STATE PRODUCTS ENGINEERING COUNCIL, "Committee Letter Ballot", JC-42.3-95-73, Item #633.13, Arlington, VA (April 1995)	
MT		YOO ET AL., "SP 23.6: A 32-Bank 1Gb DRAM with 1 GB/s Bandwidth", ISSCC96/Session 23/DRAM/PAPER SP 23.6	
		NITTA ET AL., "SP 23.6: A 1.6GB/s Data-Rate 1Gb Synchronous DRAM with Hierarchical Square-Shaped Memory Block and Distributed Bank Architecture", ISSCC96/Session 23/DRAM PAPER SP 23.5	
		U.S. Patent Application S.N. 08/521,563, entitled IMPROVED VOLTAGE REGULATOR CIRCUIT, filed 8/30/95	
		U.S. Patent Application S.N. 08/668,347, entitled DIFFERENTIAL VOLTAGE REGULATOR, filed 6/26/96	
MT		U.S. Patent Application S.N. 08/460,234, entitled SINGLE DEPOSITION LAYER METAL DYNAMIC RANDOM ACCESS MEMORY, filed 8/17/95	
		U.S. Patent Application S.N. 08/420,943, entitled DYNAMIC RANDOM-ACCESS MEMORY, filed 6/4/96	
MT		U.S. Patent Application S.N. 08/194,184, entitled INTEGRATED CIRCUIT POWER SUPPLY HAVING PIECEWISE LINEARITY, filed 2/8/94	

Examiner Signature	AL. TRAN	Date Considered	10/21/03
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² Applicant is to place a check mark here if English language translation is attached.

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		Attorney Docket Number	DB000575-010

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Examiner Initials*	Cite No.†	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), file of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume/issue number(s), publisher, city and/or country where published.	TP
DET		U.S. Patent Application S.N. 08/137,679, entitled A VOLTAGE REFERENCE CIRCUIT WITH COMMON GATE LOADING FOR A CURRENT MIRROR OUTPUT STAGE, filed 10/14/93	
AT		U.S. Patent Application S.N. 08/325,766, entitled AN EFFICIENT METHOD FOR OBTAINING USABLE PARTS FROM A PARTIALLY GOOD MEMORY INTEGRATED CIRCUIT, filed 10/19/94	

Examiner Signature	M. TRAN	Date Considered	10/21/03
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